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METHOD OF ENCAPSULATING DIE AND CHIP CARRIER

Technical Field

The present invention relates generally to a method of encapsulating a semiconductor chip assembly, and more specifically to a method of encapsulating a semiconductor chip assembly within a ring or a can, while protecting the terminals on the chip carrier.

Background of the Invention

A semiconductor chip assembly may include a chip carrier which includes a dielectric layer overlying the front surface of the chip, with an array of terminals or "bumps" on the dielectric layer, and leads electrically connected to the terminals, and a semiconductor chip or "die". The bumps in the chip carrier are connected via the leads to contacts on the die. Such a chip assembly typically is used by placing it on a circuit board or other circuit panel and electrically connecting the terminals on the chip carrier to the panel as by soldering.

It is often desirable to more effectively "package" a semiconductor chip assembly so that it can be handled with less fear of damage to the assembly so that a heat sink can be married with the semiconductor chip or both. However, if a semiconductor chip assembly is to be so packaged for these or other purposes, the utmost care must be taken during the packaging process to avoid affecting the integrity of the terminals on the chip carrier. In particular, it is important to avoid contaminating the terminals on the chip carrier with the encapsulant.

Accordingly, a method of controlling the encapsulation of a semiconductor chip assembly, with or without an elastomeric pad or layer, such that the integrity of the terminals and leads are not affected is desirable.

Summary of the Invention

The present invention provides a method of controlling encapsulation of a semiconductor chip

assembly, as well as providing a method of simultaneously forming elastomeric layer and controlling such encapsulation.

In accordance with one embodiment of the present invention, a semiconductor chip assembly or other component having a top layer with an array of exposed terminals is encapsulated by placing it in an encapsulant barrier next to the semiconductor chip assembly such that it at least partially defines an encapsulation area, and providing a protective barrier for protecting the exposed terminals on the top layer during encapsulation. Encapsulation material is introduced into the encapsulation area, and by reason of the protective barrier, it is prevented from affecting the integrity of the exposed terminals. It is noted that the present invention contemplates the employment of the steps in any suitable order.

Preferably, the encapsulation material is introduced in a liquid form, and is subsequently hardened by any suitable means of curing the encapsulation material. In another embodiment of the present invention, the encapsulation material can be disposed in the encapsulation area as a preform, either before or after the protective barriers associated with the exposed terminals and before or after the encapsulant barrier is placed adjacent to the semiconductor chip assembly. The preform of the encapsulation material can then be liquified by any suitable means so that the encapsulation material flows throughout the encapsulation area or a desired part of the encapsulation area.

In the preferred embodiment, the encapsulant barrier is at least a portion of a can which will form part of the encapsulation. The can is preferably made of a material which is high in thermal conductivity, such as aluminum. In another embodiment, however, the encapsulant barrier can be a ring which will remain as part of the encapsulation, but will not provide a heat

sinking base. In this instance, other suitable heat sinking arrangements, or none at all, might be employed. In yet another embodiment, the encapsulant barrier can merely be a mold which will be removed after encapsulation.

It may also be desirable to provide the encapsulant barrier with means for allowing the encapsulation material to flow out of the encapsulation area and away from the exposed terminals. This might be in the form of a lowered wall, a lowered wall section, or holes provided in the walls of the can or other encapsulant barrier.

The present invention also contemplates the positioning of the semiconductor chip assembly within a can or other encapsulant barrier by means of positioning or centering means in the can.

Preferably, the protective barrier utilized in the present invention is a solder mask which provides an array of terminal holes which correspond to the array of exposed terminals on the top layer of the semiconductor chip assembly. Preferably, the terminal holes are sized to tightly receive the terminals or bumps so that the terminals are surrounded by the dielectric material of which solder mask is made. However, larger terminal holes can be provided, or, in the alternative, a large opening can be provided in the solder mask so that the entire array of terminals are exposed in such large opening.

Preferably, the solder mask is vacuum laminated to the top layer of the semiconductor chip assembly. More preferably, the solder mask is vacuum laminated not only to the top layer of the semiconductor chip assembly but also to the top side of the encapsulant barrier (the top side of the can, ring or mold walls). This arrangement, in many instances and at least with respect to the use of certain cans or molds, will fully enclose the encapsulation area, although the encapsulation area need not be so defined for the

purposes of the present invention. In other words, the encapsulation area only need be partially bounded by the chip assembly, solder mask and encapsulant barrier. However, in the instance where it is fully enclosed or fully bounded by these components, it is desirable to provide a fill hole through which the encapsulation material can be injected into the encapsulation area, and in some instances, it may be preferable to utilize or provide a vent hole to prevent air from becoming entrapped in the encapsulation area.

In many instances, the encapsulation area is defined such that inversion of the encapsulant barrier, protected barrier and semiconductor assembly will facilitate the introduction of the encapsulation material.

In other embodiments of the present invention, the protective barrier can be a dam, a cap, a cover, or any other means which protects the exposed terminals on the top layer of the semiconductor chip assembly. This could also include a flexible covering member which, upon the application of pressure, will deform into engagement with the top layer around the exposed terminals to protect the same.

It should be understood that the encapsulant barrier may be provided in contact with the semiconductor chip or at a distance from the semiconductor chip, although in most cases it would be preferable to have it at a distance from the semiconductor chip. In the former instance, however, the assembly to be encapsulated may be structured such that the encapsulant barrier should be in contact with the semiconductor chip or lower section of the assembly to be encapsulated. In connection with another embodiment of the present invention, the encapsulant barrier can be spaced from the lower surface of the assembly to be encapsulated. This can be accomplished by the use of a spacer or any other suitable means.

In accordance with yet another embodiment of the present invention, a semiconductor chip assembly or other component can be encapsulated by placing an encapsulant barrier adjacent the semiconductor chip assembly, such that an encapsulation area is least partially defined, and disposing a preform of encapsulation material in or adjacent the encapsulation area. The preform is of a predetermined volume which is equal to or less than the encapsulation area, such that when the preform is liquified as part of the method the encapsulation material will not flow out of the encapsulation area to possibly affect the integrity of the exposed terminals. In this embodiment, a protective barrier is not required, although it may be employed to ensure that the encapsulation material does not contact the exposed terminals or that any of the manipulation of the assembly while practicing this method will not affect the integrity of the exposed terminals.

The encapsulant can be provided as a preform which can be liquified by heating, and hardened by cooling, either directly or permitting the material to cool on its own. It is also preferable that the preform be extruded or injection molded to the predetermined volume. The preform can be in the form of an elongated bead with a circular cross section, or any other suitable form or shape,

In still another embodiment of the present invention, a semiconductor chip assembly having a top layer with exposed terminals can be simultaneously provided with elastomeric layer and encapsulated. The matter in accordance with the present invention includes placing an encapsulation barrier adjacent the semiconductor chip assembly, such that the encapsulation barrier at least partially defines an encapsulation area, introducing an encapsulation material into the gap between the semiconductor chip and the top layer of the semiconductor chip assembly, such that the encapsulation material is disposed between the top layer and the

semiconductor chip, and introducing an encapsulation material into a portion of the encapsulation and providing a protective barrier for protecting the terminals on the top layer of the semiconductor chip assembly.

Preferably, the encapsulation material utilized to fill the gap between the top layer and the semiconductor chip in the same encapsulation material used to fill at least a portion of the encapsulation area. In this instance, the step of introducing the encapsulating material into at least a portion of the encapsulation area may be a continuation of introducing the encapsulation into at least a portion of the gap. Also preferable in this and other embodiments of the present invention, the encapsulation material is an elastomer. Still further, and in accordance with the last described method, the preferential steps of materials and components discussed above in connection with other embodiments of the present invention can also be employed in connection with this method. This last described method of simultaneously forming a layer between the top layer and semiconductor chip and encapsulating the semiconductor chip assembly preferably includes supporting the top layer above the semiconductor chip. This supporting step may be particularly important where a protective barrier is to be provided to protect the exposed terminals on the top layer of the semiconductor chip assembly.

Brief Description of the Drawings

Figure 1 is an elevational view, in partial section, illustrating a semiconductor chip assembly as it is being encapsulated within a can in accordance with one embodiment of the present invention.

Figure 2 is an elevational view, in partial section, of a semiconductor chip assembly being encapsulated within a ring in accordance with another embodiment of the present invention.

Figure 3 is an elevational view, in partial section, illustrating a semiconductor chip assembly being encapsulated in an inverted position within a ring in accordance with another embodiment of the present invention.

Figure 4 is a top plan view of a solder mask which can be used in accordance with different embodiments of the present invention.

Figure 5 is an elevational view, in partial section, illustrating the encapsulation of the semiconductor chip assembly within a can in accordance with another embodiment of the present invention.

Figure 6 is a top plan view of a semiconductor chip assembly positioned within a can having a centering structure.

Figure 7 is an elevational view, in partial section, illustrating the encapsulation of a semiconductor chip assembly in an inverted position within a can in accordance with another embodiment of the present invention.

Figure 8 is an elevational view of a semiconductor chip assembly being prepared for encapsulation within a can, illustrating in particular the use of a terminal cap or cover in accordance with another embodiment of the present invention.

Figure 9 is an elevational view, in partial section, illustrating the simultaneous formation of an elastomeric pad and the encapsulation of a semiconductor chip assembly in accordance with another embodiment of the present invention.

Figure 10A is an elevational view, in section, illustrating a ring, solder mask and preform arranged to facilitate the encapsulation of a semiconductor chip assembly in accordance with another embodiment of the present invention.

Figure 10B is an elevational view, in partial cross section, of the ring, solder mask and preform in Figure 10A, as arranged in association with a

semiconductor chip assembly in preparation for encapsulation.

Figure 10C is an elevational view, in partial section, illustrating the liquification of the preform shown in Figure 10B to encapsulate the semiconductor chip assembly within the ring.

Figure 11 is a partial elevational view, in partial section, of a preform of predetermined volume associated with a ring as it is being arranged in association with a semiconductor chip assembly for the encapsulation of such semiconductor chip assembly in accordance with another embodiment of the present invention.

Figure 12 is an elevational view, in partial section, of a semiconductor chip assembly as it is being prepared for encapsulation within a ring, illustrating in particular the use of a spacer in accordance with another embodiment of the present invention.

Figure 13 is an elevational view, in partial section, of a semiconductor chip as it is being prepared for encapsulation within a can, illustrating in particular the leads being directed inwardly from the elastomeric pad to the contacts.

Detailed Description of the Preferred Embodiments

Referring to Figure 1, a semiconductor chip assembly, generally designated as 10, includes a semiconductor chip 12 and a chip carrier 14. The chip carrier 14 is made up of a top layer 16 (preferably a polyimide layer or the like) and an elastomeric pad 20 disposed between the top layer 16 and the semiconductor chip 12. The semiconductor chip 12 and the chip carrier 14 are electrically connected via a plurality of leads 22 which are connected to the chip 12 via contacts 24. The leads 22 are electrically connected to terminals 26 which protrude as "bumps" from the top surface 18 of the chip carrier 14. This assembly may, for example, be in accordance with commonly assigned United States Patents 5,148,266; 5,258,330 and 5,148,265. The arrangement of

the leads 22 and the array of terminals 26 can be seen more clearly in the plan view of the semiconductor chip assembly 10 shown in Figure 6, although any arrangement of leads and terminals might form part of a given semiconductor chip assembly or other component to which the present invention is applicable. It is the terminals 26 which connect the semiconductor chip assembly 10 to a printed circuit board or other substrate (not shown), and thus it is critical that the integrity of the terminals 26 must be preserved throughout testing and final assembly.

The semiconductor chip assembly 10 is, in Figure 1, positioned for encapsulation within a can 28. The can 28, in this embodiment, will form part of the encapsulation, and preferably will serve as a heat sink for the semiconductor chip assembly 10. Thus, the can 28 is preferably made of a material which is high in thermal conductivity, depending upon the specific component and its application. Aluminum is preferable in most instances. The can has a surface 29 fastened to the rear or bottom face of chip 12 by thermally conductive adhesive such as a silver-filled epoxy (not shown).

Figure 1 shows the use of a solder mask 30 which is in contact with and preferably connected to the top side of the walls of can 28 and the top surface 18 of the chip carrier 14. While the solder mask 30 could merely have a large opening through which the array of terminals 26 are exposed, the solder mask 30 being connected to the perimeter of the top surface of chip carrier 14, it is preferable to provide solder mask 30 with an array of terminal holes 37 corresponding to the array of terminals 26 on the chip carrier 14. The array of terminal holes 37 is shown clearly in Figure 4. The terminal holes 37 can be registered with the terminals 26, and are preferably of such a size that the solder mask 30 must be pressed over the terminals 26. This provides a relatively tight fit of the terminals 26 in

the terminal holes of the solder mask 30. The solder mask can be attached to the top edge of the walls of can 28 and the top surface 18 of the chip carrier 14 by a vacuum lamination method, using heat and pressure to secure the solder mask 30 in place. Any other suitable method of attachment can be used. The solder mask 30 is preferably made of a dielectric material, such as a film selected from the group consisting of release film, 1/2 mil adhesive and 1/2 mil polyimide or stand-alone adhesive with release film on each side which can be vacuum laminated. Since its dielectric properties will be advantageous when the terminals 26 are employed during testing or final assembly. A photosensitive polymer film may be employed to permit formation of holes 37 by photographic processor. The preferred material for the solder mask 30 is Dupont VACREL 8100, which exhibits the desirable photosensitive and dielectric properties.

Once the semiconductor chip assembly 10 has been positioned within the can 28, and the solder mask 30 has been secured to protect the terminals 26 from the encapsulation material, the encapsulation material can be introduced into the encapsulation area, which, in most instances, about the periphery of the semiconductor chip assembly 10. This can be accomplished in a number of ways, including most preferably, the use of a needle 32 which is connected to a source 34. Thus, the needle is inserted into a fill hole 36 in the solder mask 30, there being a vent hole 38 as well, if required. The encapsulation material 40 is either injected into the encapsulation area or may, in connection with certain embodiments of the present invention, be conveyed or "pulled" from needle 32 by the capillary-like relationship of the encapsulation material 40 to the semiconductor chip assembly 10, causing the wetting of the surfaces of the semiconductor chip assembly 10. The latter method of introduction depends, of course, upon the type of encapsulation material 40 used.

The encapsulation material 40 can be of any suitable material,but preferably is a silicone resin, and in the preferred embodiment of the present invention it is a curable silicone-based encapsulant such as DC577, which is manufactured by Dow Corning Corporation of Midland, Michigan. The encapsulation material 40 can be cured or partially cured in any suitable fashion, such as exposure to radiant energy, thermal energy or ultraviolet light. Several ways in which to cure materials are disclosed in the '882 application.

Figure 2 illustrates a semiconductor chip assembly 10 as positioned within a ring 42, which is essentially a wall disposed about the periphery of the semiconductor chip assembly 10. In this case, a separate type of heat sink might be applied to the bottom surface of the chip 12 (as opposed to the bottom of the can 28 as shown in Figure 1). Thus, there is an opening between the ring 42 and the chip 12 in the arrangement shown in Figure 2. This opening might be closed for purposes of encapsulation by a mold, support surface or other substrate. In the alternative, the encapsulation material 40 might be chosen to operate on the basis of capillary action, thus wetting the surfaces and limiting and terminating flow based on surface tension (as illustrated in Figure 10C with respect to a different embodiment of the present invention). This would prevent the encapsulation material from flowing out of the encapsulation area.

Yet another alternative would be to invert the structure shown in Figure 2, but without a fill or vent hole in the solder mask 30, as shown in Figure 3. Thus, the opening between the ring 42 and the chip 12 will be used in order to fill the encapsulation area with the needle 32 or any other suitable means.

Figure 5 illustrates yet another embodiment by which the terminals 26 on the chip carrier 14 can be protected from the encapsulation material 40. In this embodiment, a peripheral dam 44, which essentially

consists of a wall disposed about the periphery of the top surface of chip carrier 14. This wall might be temporarily fixed to the top surface of the chip carrier 14, or, more preferably, will be a metal or plastic dam which is maintained in place on top of the chip carrier 14 by its own weight. The dam 44 will prevent the flow of the encapsulation material towards the terminals 26 on the chip carrier 14. Once the encapsulation area has been filled, the dam 44 can be removed. The dam 44 might also be in the form of a cap or cover which can be placed on the chip carrier 14, and subsequently removed.

The embodiment shown in Figure 8 is similar to the use of a dam 44 or a cover. It provides a shield 46 which includes an array of dimples 48 which matches the array of terminals 26. The shield 46 can be made of any suitable material. The concept of a shield can also be applied by utilizing a rubber shield which need not provide dimples 48, but rather will rely upon the deformability of the rubber material to surround and protect the terminals 26. Of course, in using such a rubber shield, some pressure must be applied in order to cause the rubber material to surround the terminals 26, particularly the terminals 26 around the periphery the chip carrier 14.

Figure 7 shows yet another embodiment of a semiconductor chip assembly 10 within a can 28 and employing a solder mask 30. In this embodiment, the needle 32 is inserted into a fill hole 29 in the can 28 while the entire assembly is in the inverted position. Again, as in the embodiment shown in Figure 1, a vent hole might be necessary in the can 28 so that air does not become trapped in the encapsulation area.

Figure 9 is yet another embodiment of the present invention by which an elastomeric layer is formed between the top layer 16 of the chip carrier 14 and the chip 12 simultaneously with the encapsulation of the semiconductor chip assembly 10. The chip carrier top layer 16 is initially connected to the chip by

bonding leads 22 to the contacts of the chip, so that the top layer is supported about the chip surface by the leads. Such a procedure is disclosed for example in U.S. Application Serial No. 08/123,882 filed on September 20, 1993 by Sweis et al. ("the '882 application"). The '882 application discloses a method of interfacing a chip carrier and a semiconductor chip, as well as providing an elastomeric layer. The disclosure of the '882 application is incorporated herein by reference, although it should be recognized that the present invention is applicable in connection with methods and semiconductor chip assemblies of any type and in addition to those disclosed in the '882 application. Initially, as in the other embodiments, the solder mask 30 is attached to the top side of the can 28 and the top surface 18 of the chip carrier 14. It is preferable, particularly when the solder mask 30 is to be vacuum laminated to the top surface of the chip carrier 14, that the chip carrier 14 be supported above the chip 12 by outer structures in addition to leads 22 so that the integrity of the leads 22 and the connection of such leads to the chip 12 and the chip carrier 14 are not affected during lamination of the solder mask 30. Supports 46, in the form of posts, are shown in Figure 9 between chip carrier 14 and chip 12. These posts are disposed on chip 12 before assembly of layer 16. The solder mask 30 is laminated to the top side of the can walls and the top surface 18 of the chip carrier 14. As in other embodiments, the solder mask 30 might include a vent hole 38 to prevent air from becoming within the encapsulation area or within the elastomeric layer area. A needle 32 is then inserted through aligned apertures in the chip carrier 14 and the solder mask 30, and the encapsulation material 40 is either injected into the gap between layer 16 and chip 12. As discussed in detail in the '882 application, the elastomeric material can convey itself through the gap area by capillary action.

Figures 10A-10C illustrate the steps taken in accordance with yet another embodiment of the present invention. Generally, this embodiment relates to the use of a preform 48 of the encapsulation material 40. In other words, the encapsulation material 40 can be arranged in or adjacent the encapsulation area in a non-liquid state, so that the encapsulation material 40 can flow into or throughout the encapsulation area upon application of heat or any other expedient appropriate for a given encapsulation material. This concept can be employed in connection with any other embodiment of the present invention, and is not limited to the specific steps shown in Figures 10A-10C.

In ~~Figure 10A~~ Figures 10A and 10B, the preform 48 is provided around the inside of a can 42 which is to surround a chip assembly 10. The can 42 has an inverted L-shaped profile in this embodiment, but can take on any appropriate shape. A solder mask 30 is provided, and includes terminal holes 37 for registration with the terminals 26 of a chip assembly 10. The solder mask 30 is secured to the top side of the can 42, by vacuum lamination or any other method of attachment, either before or after association with the chip assembly 10. The structure in Figure 10A is then married with a semiconductor chip assembly 10, the terminals 26 being pressed through the terminal holes 37. As shown in Figure 10B, the preform 48 might be deformed somewhat by the peripheral portions of the chip assembly 10.

In Figure 10C, the melting of the preform 48 and the flowing of the encapsulation material 40 is illustrated. As shown in Figure 10C, a meniscus 50 is formed in the opening between the can 42 and the assembly 10, thus preventing the encapsulation material 40 from flowing out of the encapsulation area. It is noted that the encapsulation material 40 must be, in the illustrated embodiment, one which works by capillary action and exhibits sufficient surface tension to form the meniscus and prevent the further flow of the

encapsulation material 40. On the other hand, the structure shown in Figure 10B can be inverted and the preform can be subjected to heat, thus melting the preform 48, whereupon the encapsulation material 40 will fill the encapsulation area by gravity.

The melting of the preform 48 when the structure is in the inverted position lends itself to the use of a preform 48 of a specific volume that will fill the encapsulation area, but will not overflow out of the encapsulation area. Such a preform 48 is shown in Figure 11 disposed in connection with a can 42 having an L-shaped profile. Unlike Figures 10A-10C, the structure in Figure 11 does not show the use of a solder mask or other physical barrier to protect the terminals 26. Rather, the preform 48 is of such a volume that it will fill only the encapsulation area. Of course, both measures of protecting the terminals 26 can be employed (i.e., a physical barrier and a preform of predetermined volume). Thus, the encapsulation area must be calculated, and an appropriately sized preform must be provided. The preform can be a bead of encapsulation material formed by extrusion or injection molding or any other means. It must, however, be relatively uniform in size so that an appropriate amount of encapsulation material flows in every area about the periphery of the chip assembly 10, yet does not overfill the encapsulation area at any point.

The heating of the preform in any of the previously discussed embodiments can be accomplished by heating the lower surface of the chip 12 in a vacuum oven. In order to control the flow of the encapsulation material and prevent damage to the chip carrier 14, the top of the assembly might be cooled to reduce radiant heat.

In Figure 12, a semiconductor chip assembly 10 is shown on a support surface 54, and surrounded by a ring 42. As the ring is not high enough to be flush with the top surface of the chip carrier 14, a spacer 52

is provided about the periphery of the chip assembly 10 and under the ring 42.

A further embodiment is shown in Figure 13, revealing that the present invention contemplates arrangements which differ from the arrangement set forth above. Specifically, in Figure 13, the semiconductor chip 12 is surrounded by a chip carrier 14, which is preferably formed by a top layer 16 and an elastomeric pad 20. In this case, the chip carrier 14 surrounds the semiconductor chip 12, and the leads 22 from the chip carrier 14 are directed inwardly and are connected to the semiconductor chip 12 via contacts 24. As with previous embodiments, this assembly can be encapsulated as shown in any of the previous embodiments. In Figure 13, this assembly is positioned with a can 28 for encapsulation. Although any of the previously-described methods might be suitable for encapsulating the assembly in Figure 13, the use of the solder mask 30 over the terminals or bumps 26 is illustrated. The solder mask 30 includes a fill hole 36 for purposes of inserting the encapsulation material, as well as a vent hole 38.

The present invention can be applied in encapsulating any structure, whether the leads fan in, fan out or both. Any of the structure and arrangements illustrated and described in commonly assigned U.S. Patent No. 5,148,265, the disclosure of which is incorporated herein by reference, can be encapsulated in accordance with the present invention.

While the foregoing description and figures illustrate some preferred embodiments of the method in accordance with the present invention, it should be appreciated that certain modifications may be made and are encouraged to be made in the steps, structure, arrangement and materials of the disclosed embodiments, particularly as may be applicable from the disclosure incorporated herein by reference, without departing from the spirit and scope of the present invention which is

defined by the claims which are set forth immediately hereafter.